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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/711,511 | 09/23/2004 | Sheng Wu | 13040-US-PA | 5510 |

31561 7590 08/16/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

| EXAMINER | |
|---|---|
| TSAI, H JEY | |
| **ART UNIT** | **PAPER NUMBER** |
| 2812 | |

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/711,511 | WU ET AL. |
| | Examiner | Art Unit |
| | H.Jey Tsai | 2812 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, 15-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lin et al. 6,249,022.

Lin et al. discloses a method of manufacturing a non-volatile memory cell, comprising:

forming a first dielectric layer (a tunneling oxide) 212 over a substrate, fig. 3A and col. 3, lines 13-67,

forming a second dielectric layer 214 having a trench over the first dielectric layer 212,

forming a pair of charge storage spacers 202 on sidewalls of the trench,

forming a third dielectric layer 224 over the substrate to cover the first dielectric layer, the charge storage spacers 202 and the second dielectric layer 214,

forming a conductive structure 222 on a position over the charge storage spacers on the third dielectric layer,

removing portions of the third dielectric layer 224, the second dielectric layer 214 and first dielectric layer not covered by the conductive structure 204,

forming source/drain regions 206 in the substrate at each side of the conductive structure 204,

wherein the first dielectric layer 212 comprises a silicon oxide layer, col. 3, lines 15-20,

wherein forming the pair of charge storage spacers on the sidewalls of the trench comprises: forming a charge storage material layer over the substrate, and etching back the charge storage material layer, fig. 3B, col. 3, lines 22-67,

wherein an etching selectivity of the charge storage material layer (silicon nitride) has different etching selectivity from the second dielectric layer (silicon oxide), col. 3, lines 40-67.

***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,635,533. Although the conflicting claims are not identical, they are not patentably distinct from each other because pad oxide layer is equivalent to first dielectric layer and omitting forming a tunneling oxide layer within the opening in the claimed invention is obvious.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. 2004/0207007 in view of Lin et al. 6,249,022.

The reference(s) teach the features:

Lin et al. discloses a method of manufacturing a non-volatile memory cell, comprising:

forming a tunneling dielectric layer (a tunneling oxide) 120 over a substrate 100, fig. 2A and para. 38,

forming a patterned dielectric layer 130 having a trench over the first dielectric layer 120,

forming a pair of conductive charge storage spacers 175 on sidewalls of the trench, fig. 2g and para. 42,

forming an inter-gate dielectric layer 180 over the substrate to cover the tunneling dielectric layer 120, the charge storage spacers 175 and the patterned dielectric layer 130,

forming a conductive structure 190/195 on a position over the conductive charge storage spacers 175 on the third dielectric layer 180,

removing portions of the inter-gate dielectric layer 180, the second dielectric layer 130 and first dielectric layer not covered by the conductive structure 195,

forming source/drain regions 105 in the substrate at each side of the conductive structure,

wherein the first dielectric layer 120 comprises a silicon oxide layer, para. 39,

wherein forming the pair of conductive charge storage spacers 175 on the sidewalls of the trench comprises: forming a conductive charge storage material layer 170 over the substrate, and etching back the charge storage material layer, fig. 2i-2h,

wherein an etching selectivity of the charge storage material layer (polysilicon) has different etching selectivity from the second dielectric layer (silicon nitride), para. 39-42.

The difference between the reference(s) and the claims are as follows: Lin et al. '007 teaches removing the inter-gate dielectric layer and a patterned dielectric layer but does not teach removing the tunneling layer. However, Lin et al. '022 teaches at fig. 3D, removing the tunneling oxide layer 220.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Lin's '007 process by removing the tunneling layer as suggested by Lin et al. '022 because source/drain ion implantation can directly implant into substrate without going through tunneling oxide layer.

Claims 6-7 and 18 are rejected under 35 U.S.C 103 as being unpatentable over Lin et al. as applied to claims 1-5, 8, 15-17 above, and further in view of Lin et al. 2004/0207007.

The difference between the references applied above and the instant claim(s) is: Lin et al. '022 teaches forming a silicon nitride charge storage spacers but does not

teach using a polysilcon as a charge storage spacer and annealing. However, Lin et al. '007 teaches at para. 42, using polysilion layer 170 to form a charge storage polysilicon spacer 175 and annealing the structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by using a polysilcion charge storage spacer as taught by Lin et al. '007 because polysilcon spacer is not layer can store the charges but also is a conductor for making contact to outside the device area.

***Allowable Subject Matter***

Claims 9 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims for the reasons of forming a pair of dielectric spacers on sidewalls of the conductive structure before removing portions of the third dielectric layer, the second dielectric layer and first dielectric layer not covered by the conductive structure.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873.

The fax phone number for this Group is 571-273-8300.

hjt

8/13/2005

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800